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EXAMINER	
JAGAN, MIRELLYS	
ART UNIT	**PAPER NUMBER**
2859	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/673,234	BREINLINGER, RICHARD H.	
	Examiner	Art Unit	
	Mirellys Jagan	2859	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *21-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *21-33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 September 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the "binary processor" claimed in claim 23 and the "means for producing a binary output" claimed in claim 30 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Objections

2. Claims 23, 25, 30, 32, and 33 are objected to because of the following informalities:

In claim 23, there is lack of antecedent basis in the specification for the system having "a binary processor".

In claim 25, there is lack of antecedent basis in the claim for "the second processor unit" in line 2.

In claim 29, there is lack of antecedent basis in the claim for "the controller" in line 8.

In claim 30, there is lack of antecedent basis in the specification for the system having "means for producing a binary output".

In claim 32, there is lack of antecedent basis in the claim for "the controller" in line 2.

Claim 33 is objected to for being dependent on objected base claim 32. Appropriate correction is required.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 23 and 29-33 are rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01.

In claim 23, the omitted structural cooperative relationship is between the binary processor and the processor unit. It is not clear how the binary processor and the processor unit are structurally related to each other, i.e., is the binary processor a part of the processor unit, or is it a separate processor from the processor unit? Furthermore, it is not clear from the specification how the binary processor and the processor unit are structurally related to each other since there is lack of antecedent basis in the disclosure for a "binary processor".

In claim 29, the omitted structural cooperative relationship is between the means for determining a temperature proximate the diode and the processor unit. The specification discloses that the processor unit has the means for determining a temperature proximate the diode. Therefore, claim 29 lacks structural relationship between the means and the unit since it is stating that the temperature proximate the diode is determined by means other than the means of the processor unit.

Claims 30-33 are rejected for being dependent on rejected base claim 29.

Double Patenting

5. A rejection based on double patenting of the "same invention" type finds its support in the language of 35 U.S.C. 101 which states that "whoever invents or discovers any new and useful process ... may obtain a patent therefor ..." (Emphasis added). Thus, the term "same invention," in this context, means an invention drawn to identical subject matter. See ***Miller v. Eagle Mfg. Co.***, 151 U.S. 186 (1894); ***In re Ockert***, 245 F.2d 467, 114 USPQ 330 (CCPA 1957); and ***In re Vogel***, 422 F.2d 438, 164 USPQ 619 (CCPA 1970).

A statutory type (35 U.S.C. 101) double patenting rejection can be overcome by canceling or amending the conflicting claims so they are no longer coextensive in scope. The filing of a terminal disclaimer cannot overcome a double patenting rejection based upon 35 U.S.C. 101.

6. Claim 29 is rejected under 35 U.S.C. 101 as claiming the same invention as that of claim 1 of prior U.S. Patent No. 6,679,628. This is a double patenting rejection.

Claim 29 claims the same invention as claim 1 since the PLC of claim 1 is inherently a processor unit.

7. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See ***In re Goodman***, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); ***In re Longi***, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); ***In re Van Ornum***, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); ***In re Vogel***, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and ***In re Thorington***, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

8. Claims 21 and 26 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 18 of U.S. Patent No. 6,679,628.

Claim 18 claims a system having a PLC; a temperature measurement diode; an integrated circuit coupled to the diode and the PLC, the circuit comprising a analog-to-digital converter configured to sequentially digitize analog voltage signals provided by the diode; a current source coupled to the diode and configured to generate a first current and a second current different from the first current; a processor coupled to the current source and the converter and configured to control the current source such that the source sequentially applies the first current to the diode at a first point in time and applies the second current to the diode at a second point in time, to obtain a digital measure of a first voltage across the diode from the converter when the first current is applied to the diode, to obtain a digital measure of a second voltage across the diode from the converter when the second current is applied to the diode, and determine the temperature proximate the diode based on the first and second digital measures; and a temperature unit configured to host the converter and current source.

Claim 18 does not claim the system without the PLC.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify claim 18 by claiming the system without the PLC in order to minimize the number of parts in the system, and since the operation of the system will not be modified by not having the PLC.

9. Claim 22 is rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 14 of U.S. Patent No. 6,679,628.

Claim 14 claims a system having a PLC; a temperature measurement diode; an integrated circuit coupled to the diode and the PLC, the circuit comprising a analog-to-digital

converter configured to sequentially digitize analog voltage signals provided by the diode; a current source coupled to the diode and configured to generate a first current and a second current different from the first current; and a processor coupled to the current source and the converter and configured to control the current source such that the source sequentially applies the first current to the diode at a first point in time and applies the second current to the diode at a second point in time, to obtain a digital measure of a first voltage across the diode from the converter when the first current is applied to the diode, to obtain a digital measure of a second voltage across the diode from the converter when the second current is applied to the diode, and determine the temperature proximate the diode based on the first and second digital measures; wherein the processor is contained within the PLC.

Claim 14 does not claim that the PLC hosts the processor.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify claim 14 by claiming the PLC 'hosts' the processor since the PLC of claim 14 inherently 'hosts' the processor by containing it therein.

10. Claim 23 is rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 18 of U.S. Patent No. 6,679,628 in view of U.S. Patent 4,123,938 to Hamilton.

Claim 18 claims a system having all of the limitations of claim 23, as stated above in paragraph 8, except for the system further comprising a binary processor configured to generate and output a binary signal corresponding to the determined temperature.

Hamilton discloses a system for measuring temperatures using a diode as a temperature sensor. Hamilton teaches that it is useful to provide a binary processor configured to generate a binary signal corresponding to a digital temperature signal in order to display the temperature.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the system claimed in claim 18 by claiming that the system also has a binary processor, as taught by Hamilton, since Hamilton teaches that it is useful to use a binary processor to display the temperature.

11. Claims 24 and 25 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 14 of U.S. Patent No. 6,679,628 in view of claim 17 of U.S. Patent No. 6,679,628.

Claim 14 claims a system having all of the limitations of claim 24, as stated above in paragraph 9, except for the system further comprising an I/O module external to the controller and configured to couple the controller to the converter and the current source, wherein the processor is contained in the I/O module.

Claim 17 claims a system wherein the I/O module is external to the PLC and configured to couple the PLC to the converter and the current source, wherein the processor is contained in the I/O module.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the system claimed in claim 14 by claiming that the system further has an I/O module external to the controller and configured to couple the controller to the converter and the current source wherein the processor is contained in the I/O module, as

claimed in claim 17, since claim 17 teaches that it is useful to couple the controller to the converter and the current source using an I/O module containing the processor.

12. Claim 27 is rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 14 of U.S. Patent No. 6,679,628 in view of claim 13 of U.S. Patent No. 6,679,628.

Claim 14 claims a system having all of the limitations of claim 27, as stated above in paragraph 9, except for the system further comprising an I/O module external to the controller and configured to host the converter and the current source.

Claim 13 claims a system wherein the I/O module is external to the controller and is configured to host the converter and the current source.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the system claimed in claim 14 by claiming that the system further has an I/O module external to the controller and configured to host the converter and the current source, as claimed in claim 17, since claim 17 teaches that it is useful to use the I/O module as a host to the converter and the current source.

13. Claim 28 is rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 20 of U.S. Patent No. 6,679,628.

Claim 20 claims a method for automated temperature measurement comprising the steps of controlling a current source such that the source applies a first current to a diode at a first point in time and applies a second current to the diode at a second point in time; measuring a first

analog voltage across the diode when the first current is applied to the diode to produce a first analog voltage measure, and measuring a second analog voltage across the diode when the second current is applied to the diode to produce a second analog voltage measure, and sequentially digitizing the first and second analog voltage measures with an integrated circuit comprising an analog to digital converter; and determining a temperature proximate the diode based on the first and second digitized voltage measures, wherein the system comprises a PLC coupled to the converter.

Claim 20 does not claim the method without having the PLC.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify claim 20 by claiming the system without the PLC in order to minimize parts and since the method steps of the claim will not be modified by not having the PLC as part of the system.

14. Claim 30 is rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 1 of U.S. Patent No. 6,679,628 in view of Hamilton.

Claim 1 claims a system having all of the limitations of claim 30, as stated above in paragraph 6, except for the system further comprising means for producing a binary output corresponding to the determined temperature.

Hamilton discloses a system for measuring temperatures using a diode as a temperature sensor. Hamilton teaches that it is useful to provide a binary processor configured to generate a binary signal corresponding to a digital temperature signal in order to display the temperature.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the system claimed in claim 1 by claiming that the system also has means for producing a binary output corresponding to the determined temperature, as taught by Hamilton, since Hamilton teaches that it is useful to use a binary processor to display the temperature.

15. Claim 31 is rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 2 of U.S. Patent No. 6,679,628.

Claim 2 claims a system comprising a PLC, which hosts a processor; a temperature measuring diode; a current source; means for controlling the current source such that the source applies a first current to the diode at a first point in time and applies a second current to the diode at a second point in time, the means being coupled to the PLC and the current source; means for measuring a first analog voltage across the diode when the first current is applied to the diode and for measuring a second analog voltage across the diode when the second current is applied to the diode; means for sequentially digitizing the first and second analog voltage measurements with an integrated circuit; and means for determining the temperature proximate the diode based on the first and second digitized measures; wherein the PLC is configured to host the means for controlling the current source and the means for determining temperature.

16. Claims 32 and 33 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 1 of U.S. Patent No. 6,679,628 in view of claim 6 of U.S. Patent No. 6,679,628.

Claim 1 claims a system having all of the limitations of claims 32 and 33, as stated above in paragraph 6, except for the system further comprising an I/O module external to the controller and configured to couple the controller to the current source, wherein the I/O module is configured to host the means for determining temperature.

Claim 6 claims a system wherein the I/O module external to the controller and configured to couple the controller to the current source, wherein the I/O module is configured to host the means for determining temperature.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the system claimed in claim 1 by claiming that the system further comprising an I/O module external to the controller and configured to couple the controller to the current source, wherein the I/O module is configured to host the means for determining temperature, as claimed in claim 6, since claim 6 teaches that it is useful to couple the controller to the converter using an I/O module hosting the temperature measuring means.

Claim Rejections - 35 USC § 102

17. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

18. Claims 28 and 29 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent 5,195,827 to Audy et al [hereinafter Audy].

Referring to claim 28, Audy discloses a method for measuring temperature by:

controlling a current source such that the source applies a first current to a diode at a first point in time and applies a second current to the diode at a second point in time;

measuring a first analog voltage across the diode when the first current is applied to the diode to produce a first analog voltage measure, and measuring a second analog voltage across the diode when the second current is applied to the diode to produce a second analog voltage measure, and sequentially digitizing the first and second analog voltage measures with an integrated circuit comprising an analog to digital converter (26); and

determining a temperature proximate the diode based on the first and second digitized voltage measures.

Referring to claim 29, Audy discloses a system comprising:

a temperature measuring diode (22);

a curent source;

a processor unit (36) coupled to the current source and having means for controlling the current source such that the source applies the first current at a first point in time and applies the second current at a second point in time;

an analog-to-digital converter (digital voltmeter 26) for measuring a first analog voltage across the diode when the first current is applied to the diode and for measuring a second analog voltage across the diode when the second current is applied to the diode, and for sequentially digitizing the first and second analog voltage measurements with an integrated circuit; and

wherein the processor unit has means for determining a temperature proximate the diode based on the first and second digitized measures.

Claim Rejections - 35 USC § 103

19. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

20. Claims 21, 28, and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 6,554,469 to Thomson et al [hereinafter Thomson] in view of Audy.

Referring to claims 21 and 28, Thomson discloses a system comprising:

a processor unit (26);

a temperature measuring transistor (10);

an integrated circuit coupled to the diode and the processor unit, the circuit comprising an analog-to-digital converter (24) configured to sequentially digitize analog voltage signals provided by the transistor; and

a current source coupled to the transistor and configured to generate a first current (I1) and a second current (I2) different from the first current;

wherein the processor unit is coupled to the current source and the converter, and is configured to:

control the current source such that the source applies the first current at a first point in time and applies the second current at a second point in time,

obtain a digital measure of a first voltage across the transistor from the converter when the first current is applied to the transistor,

obtain a digital measure of a second voltage across the transistor from the converter when the second current is applied to the transistor, and

determine a temperature proximate the transistor based on the first and second digital measures (see figures 1 and 4; column 4, lines 35-59; and column 5, lines 1-6).

Thomson does not disclose the system using a diode as the temperature sensor.

Audy discloses a system for measuring temperature. The system comprises a diode or a transistor (22) as the temperature sensor, and a current source coupled to the diode and configured to generate a first current (I1) and a second current (I2) different from the first current, which is used by processing means to calculate the temperature. Audy teaches that a diode and a transistor are alternate and equivalent p-n junctions useful as a temperature sensor in the system (see figure 4; column 6, lines 14-16 and 39-62).

Referring to claims 21 and 28, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the system disclosed by Thomson by replacing the transistor with the diode disclosed by Audy, since Audy teaches that these elements are alternate and equivalent means for detecting temperature in the system.

Further referring to claim 28, in using the system disclosed by Thomson and Audy above to measure temperature, the method steps of claim 28 will inherently be followed.

Referring to claim 29, Thomson discloses a system comprising:

a temperature measuring transistor (10);

a curent source;

a processor unit (26) coupled to the current source and having means for controlling the current source such that the source applies the first current at a first point in time and applies the second current at a second point in time;

an analog-to-digital converter (24) for measuring a first analog voltage across the transistor when the first current is applied to the transistor and for measuring a second analog voltage across the transistor when the second current is applied to the transistor, and for sequentially digitizing the first and second analog voltage measurements with an integrated circuit; and

wherein the processor unit has means for determining a temperature proximate the transistor based on the first and second digitized measures.

Thomson does not disclose the system using a diode as the temperature sensor.

Audy discloses a system for measuring temperature. The system comprises a diode or a transistor (22) as the temperature sensor, and a current source coupled to the diode and configured to generate a first current (I1) and a second current (I2) different from the first current, which is used by processing means to calculate the temperature. Audy teaches that a diode and a transistor are alternate and equivalent p-n junctions useful as a temperature sensor in the system (see figure 4; column 6, lines 14-16 and 39-62).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the system disclosed by Thomson by replacing the transistor with the diode disclosed by Audy, since Audy teaches that these elements are alternate and equivalent means for detecting temperature in the system.

21. Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Audy in view of Thomson.

Audy discloses a system comprising:

a processor unit (36);

a temperature measurement diode (22);

an integrated circuit coupled to the diode and the processor unit, the circuit comprising a digital to analog converter (40) configured to sequentially convert digital signals from a digital voltmeter (26) into analog signals, wherein the voltmeter digitizes analog voltage signals provided by the diode; and

a current source coupled to the diode and configured to generate a first current (I1) and a second current (I2) different from the first current;

wherein the processor unit is coupled to the current source and the converter, and is configured to:

control the current source such that the source applies the first current at a first point in time and applies the second current at a second point in time,

obtain an analog measure of a first voltage across the diode from the converter when the first current is applied to the diode,

obtain an analog measure of a second voltage across the diode from the converter when the second current is applied to the diode, and

determine a temperature proximate the diode based on the first and second analog measures (see figure 4; column 6, lines 14-16 and 39-62).

Audy does not disclose the voltmeter providing the digital signals directly to the processor unit, wherein the processor unit uses the digital voltage signals to determine the temperature.

Thomson discloses a system for measuring temperature. The system comprises a p-n junction temperature sensor (10) and a current source coupled to the sensor and configured to generate a first current (I1) and a second current (I2) different from the first current to the sensor. The system has a circuit to convert the analog voltage signals from the sensor into a digital signal, and a processor unit that obtains the digital voltage signals and uses the digital signals to calculate the temperature (see figures 1 and 4; column 4, lines 35-59; and column 5, lines 1-6).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the system disclosed by Audy by replacing the processor unit and the DAC with a digital processor, as taught by Thomson, in order to process the digital signals directly from the digital voltmeter and thereby minimize the number of parts in the system and reduce manufacturing costs.

22. Claims 23 and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Thomson and Audy, as applied to claims 21, 28, and 29 above, and further in view of Hamilton.

Thomson and Audy disclose a system having all of the limitations of claims 23 and 30, as stated above in paragraph 20, except for the system comprising a binary processor configured to generate a binary signal corresponding to the temperature.

Hamilton discloses a system for measuring temperatures using a diode as a temperature sensor. Hamilton teaches that it is useful to provide a binary processor configured to generate a binary signal corresponding to a digital temperature signal in order to display the temperature.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the system disclosed by Thomson and Audy by adding a binary processor, as taught by Hamilton, in order to display the temperature.

23. Claim 23 is rejected under 35 U.S.C. 103(a) as being unpatentable over Audy and Thomson, as applied to claim 21 above, and further in view of Hamilton.

Audy and Thomson disclose a system having all of the limitations of claim 23, as stated above in paragraph 21, except for the system comprising a binary processor configured to generate a binary signal corresponding to the temperature.

Hamilton discloses a system for measuring temperatures using a diode as a temperature sensor. Hamilton teaches that it is useful to provide a binary processor configured to generate a binary signal corresponding to a digital temperature signal in order to display the temperature.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the system disclosed by Audy and Thomson by adding a binary processor, as taught by Hamilton, in order to display the temperature.

24. Claim 30 is rejected under 35 U.S.C. 103(a) as being unpatentable over Audy in view of Hamilton.

Audy discloses a system having all of the limitations of claim 30, as stated above in paragraph 18, except for the system comprising means for producing a binary output corresponding to the temperature.

Hamilton discloses a system for measuring temperatures using a diode as a temperature sensor. Hamilton teaches that it is useful to provide a binary processor configured to generate a binary signal corresponding to a digital temperature signal in order to display the temperature.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the system disclosed by Audy by adding a binary processor, as taught by Hamilton, in order to display the temperature.

Allowable Subject Matter

25. Claims 22, 24, 26, and 27 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims, and upon the filing of a terminal disclaimer in compliance with 37 CFR 1.321(c).

26. Claim 25 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims, and amended to overcome the objections set forth in this Office action, and upon the filing of a terminal disclaimer in compliance with 37 CFR 1.321(c).

27. Claims 32 and 33 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, and the objections set forth in this Office action and to include all of the limitations of the base claim and any intervening claims, and upon the filing of a terminal disclaimer in compliance with 37 CFR 1.321(c).

28. Claim 31 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims, and upon the filing of a terminal disclaimer in compliance with 37 CFR 1.321(c).

29. The following is a statement of reasons for the indication of allowable subject matter:

The prior art of record does not disclose or suggest the following in combination with the remaining limitations of the claims:

A system for automated temperature measurement, the system further comprising:

a controller configured to host the processor unit (see dependent claim 22);

an I/O module external to the controller and configured to couple the controller to the A/D converter and to the current source (see dependent claim 24);

a temperature unit is configured to host the diode, converter, and current source (dependent claim 26);

an I/O module external to the controller and configured to host the converter and the current source (dependent claim 27);

a controller configured to host the processor unit, the means for controlling the current source, and the means for determining temperature (dependent claim 31);

an I/O module external to the controller and configured to couple the controller to the current source (dependent claim 32).

Conclusion

30. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

The following patents and publications disclose temperature-sensing circuits:

U.S. Patent 4,636,092 to Hegyi

U.S. Patent 3,812,717 to Miller et al

U.S. Patent 6,097,239 to Miranda, Jr. et al

U.S. Patent 5,918,982 to Nagata et al

U.S. Patent 5,024,535 to Winston, Jr.

31. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mirellys Jagan whose telephone number is 571-272-2247. The examiner can normally be reached on Monday-Thursday from 8AM to 4PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Diego Gutierrez can be reached on 571-272-2245. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MJ
March 18, 2004

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